Debug Port Requirements for Mobile Pentium® II/III Processors

An Application Note

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The following is American Arium's recommendation for implementation of a Pentium® II target debug port.

Debug Port Signal Description

Signal	Pin	Dir	Description	Suggested Termination
TDO	10	O	TAP Data Out (From processor to ITP port)	150Ω to VCC
TDI	8	I	TAP Data In (ITP port to processor)	150Ω to VCC
TMS	7	I	TAP Mode Select	See below Note 1
TCK	5	I	TAP Clock. Of the ITP signals, this is the most critical signal.	See below Note 1
TRST#	12	I	TAP Reset	470Ω to ground
BSEN#	14	I	Boundary scan (TAP) enable. ICE has access to TAP signals of CPU when low	See below Note 5
PRDY0#	18	O	Processor PRDY signal. From 1st processor in single/multiprocessor system.	See below Note 2
PRDY1#	22	O	Processor PRDY signal. From 2nd processor (unused in a single processor system).	1KΩ to VCC
PRDY2#	26	O	Processor PRDY signal. From 3rd processor (unused in a single processor system).	1KΩ to VCC
PRDY3#	30	O	Processor PRDY signal. From 4th processor (unused in a single processor system).	1KΩ to VCC
PREQ0#	16	I	Processor PREQ signal. To 1st processor in a single/multiprocessor system.	See below Note 3
PREQ1#	20	I	Processor PREQ signal. To 2nd processor (unused in a single processor system).	No Connection
PREQ2#	24	I	Processor PREQ signal. To 3rd processor (unused in a single processor system).	No Connection
PREQ3#	28	I	Processor PREQ signal. To 4th processor (unused in a single processor system).	No Connection
RESET#	1	O	Processor RESET signal.	See below Note 4
DBRESET#	3	I	ICE reset output. When driven low, the target should reset the system and CPU.	240Ω to VCC
DBINST#	11	I	ICE installed. Debug cable grounds this signal, allowing target to detect the ICE.	See below Note 5
VTT	9	O	Target VTT. The ICE uses this to detect target power and establish GTL+ threshold.	1KΩ to VTT
BCLK	29	O	Private copy of BCLK that allows the ICE to provide a TCK that is synchronous with BCLK. In virtually all cases, a synchronous TCK is NOT used or required.	Best connected to Gnd in most cases
GND	2, 4, 6, 13, 15, 17, 19, 21, 23, 25, & 27		Signal grounds. Pin 2 (or sometimes 13) is unique in that it is sensed to determine if a target is attached.	Connect to ground

The resistor values given are typical values. Actual values are dependent on the target layout.

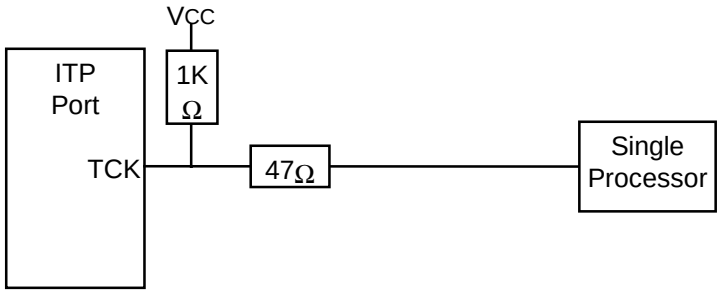
Dir (Signal Direction) is relative to target board. O (Out) is from target to ITP port. I (In) is from ITP port to target.

The Debug Port connection is achieved by way of a 30-pin connector specified as an AMP 104068-3. The pinout and suggested circuitry are fully described in the 1995 edition of the Pentium® Pro Processor Family User's Manual, Volume 1: Specifications, chapters 10 and 16 from Intel Corporation.

The Joint Test Action Group (JTAG) bus for on-module testing is defined in "Test Access Port and Boundary-Scan Architecture, IEEE 1149.1-1990, 21 May 1990."

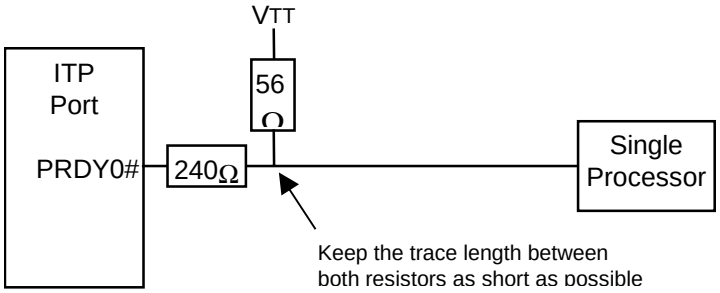
Note 1:

TCK is the most critical of the ITP signals. This note also applies to TMS. In the case of a single processor, TCK and TMS may be pulled up to VCC through a 1K ohm resistor and then passed through a 47 ohm series resistor before being routed to the processor as shown in the following figure.



Note 2:

The PRDY0# is a GTL+ signal and should be end terminated to VTT through a 56Ω resistor on the target. The signal supplied to the debug port should pass through a 240 ohm series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of this trace. The end termination resistor value for this GTL signal varies according to the effective trace impedance and VTT power dissipation issues.

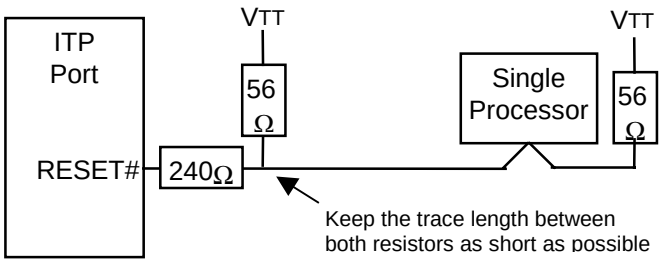


Note 3:

The PREQ0# signal should be pulled up to VCC in the range of 270 ohms to 10K ohms on the target.

Note 4:

RESET# is a GTL+ signal and should be terminated to VTT through 56Ω resistors at both ends of the signal. The signal supplied to the debug port should pass through a 240 ohm series resistor located as close as possible to the pull-up resistor. Do not add any stubs off of this trace.



Note 5:

BSEN# and DBINST# should be pulled up to VCC with a 10K resistor if this signal is used by the target. Otherwise, it may be left open.

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